Sensor-Electronics 3D Integration – Status and Possibilities

Ronald Lipton

The Technological Roadmap

Sensor integration with electronics is at the heart of modern experimental HEP. There is a continuing revolution in this area - driven by commercial applications. 3D integration is an area of great promise – well aligned to HEP needs. substantial progress can be made. It is *commercially* mature.

No new results presented – a survey of technological developments, prospects, current status and some history.

It is one part of this wide front of sensor and electronics development:

- 3D integration of electronics and sensors
- Interposers, chiplets and other interconnect technology
- Substrate engineering, LGADs, photodetectors, CCD variants
- Monolithic active pixel detectors, stitching
- SPADs, LGADs and other amplifying structures
- Radiation hard materials and structures
- Mechanics and cooling

There is a bonanza of emerging technologies … We can utilize them separately or in combination to advance experimental physics

3D Integration

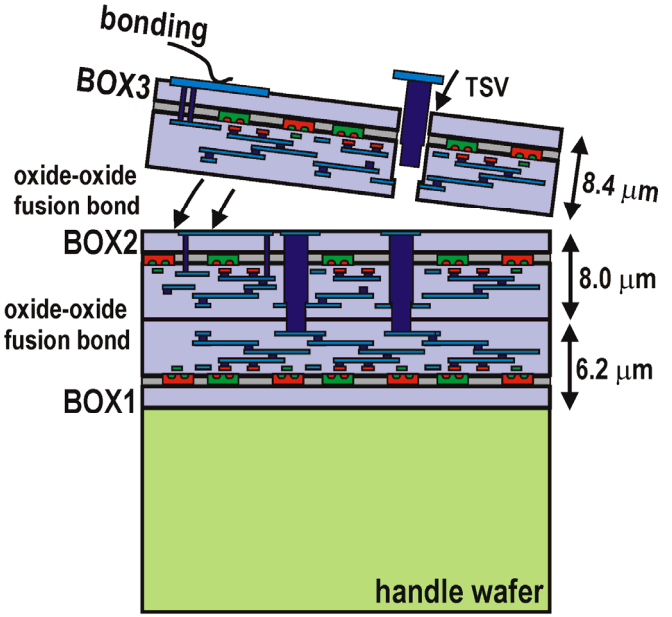
A three-dimensional integrated circuit (3D-IC) structure is composed of two or more layers of active electronic and sensor components. Enabling technologies include:

- Through-silicon vias (first, middle, last)
- Wafer-wafer or chip-wafer bonding
- Precise wafer thinning (CMP ~ few nm) and alignment

Widely adopted for imaging applications (in your iphone)

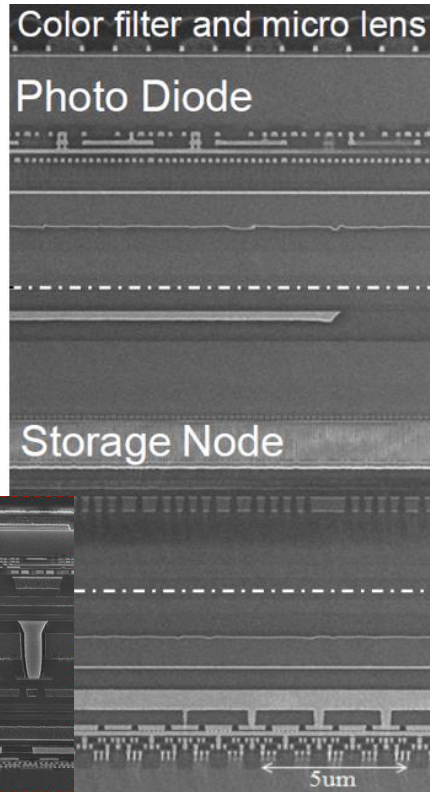
For HEP:

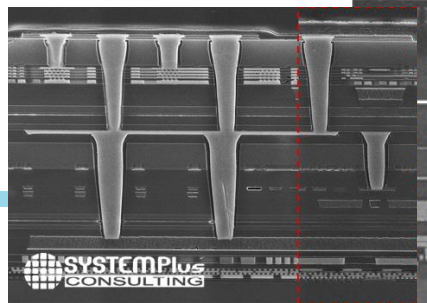
- Enables intimate interconnection between sensors and readout circuits, innovative circuit/sensor topologies
- Separate digital/analog/ and data communication tiers
- Multi-layer micro/macro pixel designs which can provide high resolution with minimal circuitry
- Wafer thinning enables thin, low mass, high resolution, and radiation hard sensors
- Bonding technologies enable very fine pitch, low capacitance, high resolution pixelated devices



Sony IMX400 3-layer stacked imager

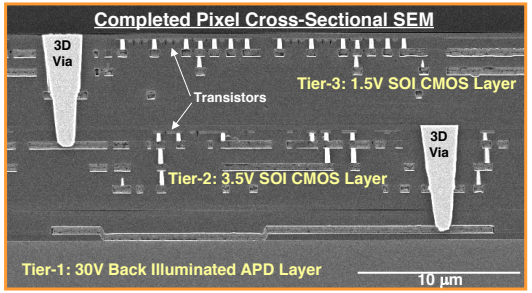
Bond layer

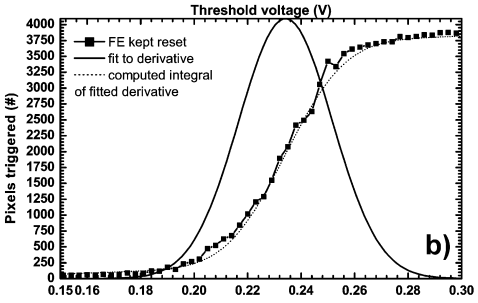




Some FNAL History – Starting with ILC Vertex R&D

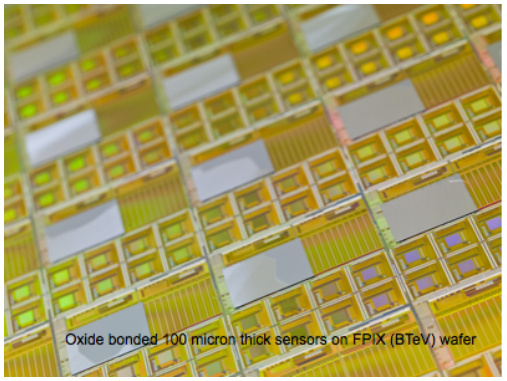
2006 - Found MIT-LL was developing a 3D process that met all the aggressive ILC vertex goals. Fabricated prototype VIP devices for DARPA-funded run. 2 Runs.

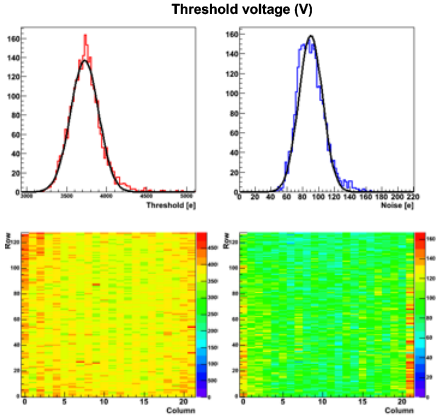




Threshold curve

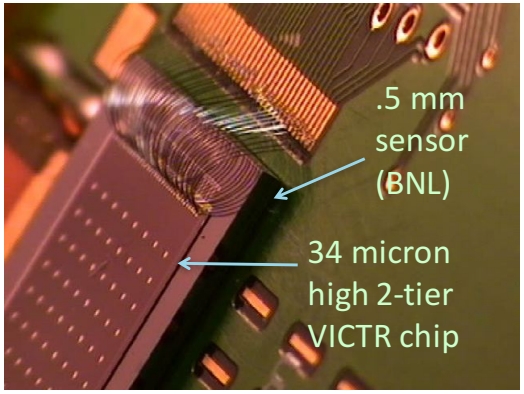
We became aware of a promising bonding technology @ Ziptronix – our initial study used old BTEV wafers with MIT-LL sensors bonded to the top layer – worked well





Threshold and noise Pixel maps

We began a major effort with int. colleagues with Tezzaron – cu-cu 3D bonding + Ziptronix sensor integration – a long haul – but the Ziptronix technology was successful. FNAL designed 3 chips – CMS, ILC, X-ray all integrated to BNL sensors



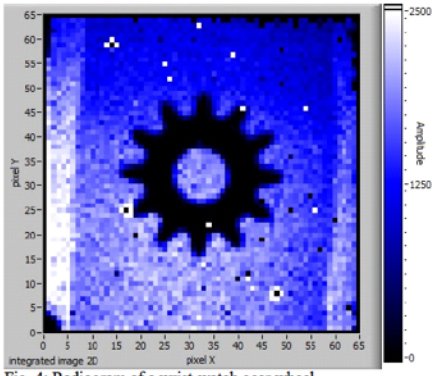


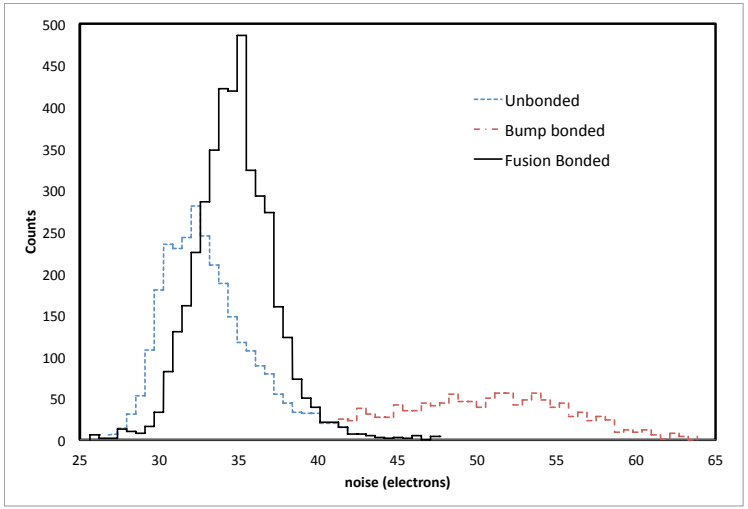
Fig. 4: Radiogram of a wrist-watch gear wheel.

VIPIC watch gear

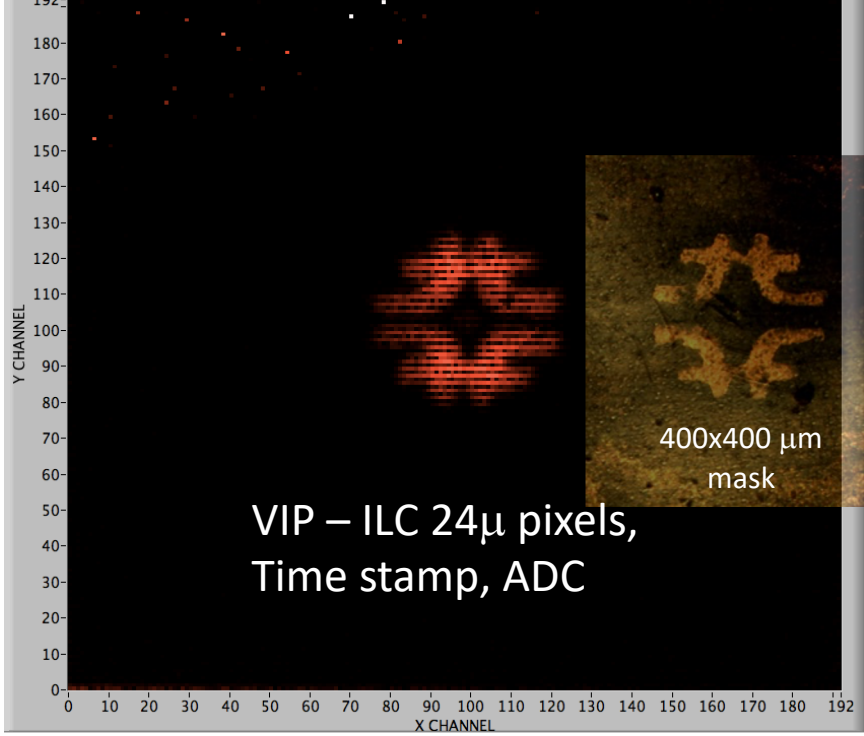
Plus studies of monolithic SOI (KEK, ASI), Laser anneal (Cornell), interposers, active edge

3D Test Results – circa 2011

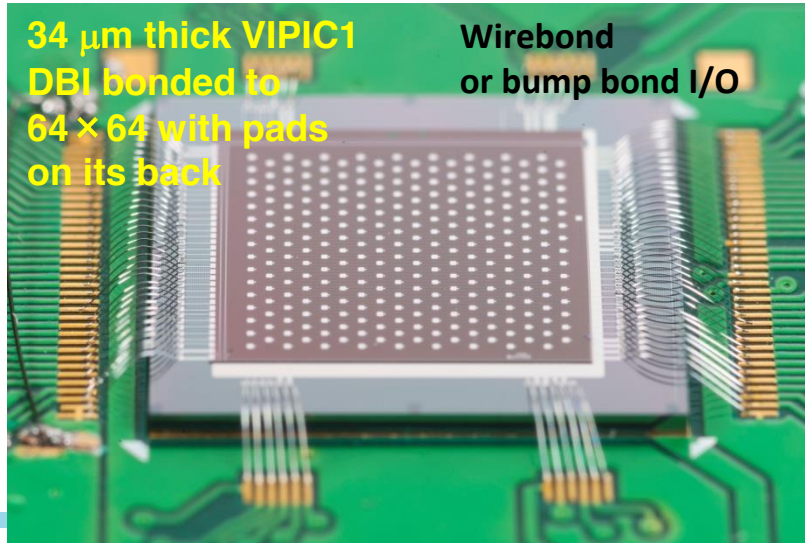
- All three 3D Chips worked – VIP (ILC) and VICTR (CMS) tested on the bench. VIPIC was extensively tested in particle and x-ray beams.
- Yields were about 50% - 3D bonding and multiple tier assembly



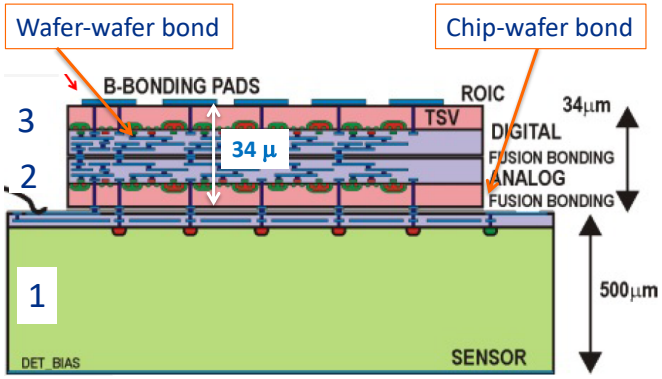
For the VIPIC x-ray imaging chip we were able to compare noise of the oxide-bonded pixels to the same chip with bump bonds. The noise in the oxide bonded pixels is almost a factor of two lower than the conventionally bump bonded parts due to lower capacitance.



CD109 radiogram of tungsten mask



It wasn't easy …



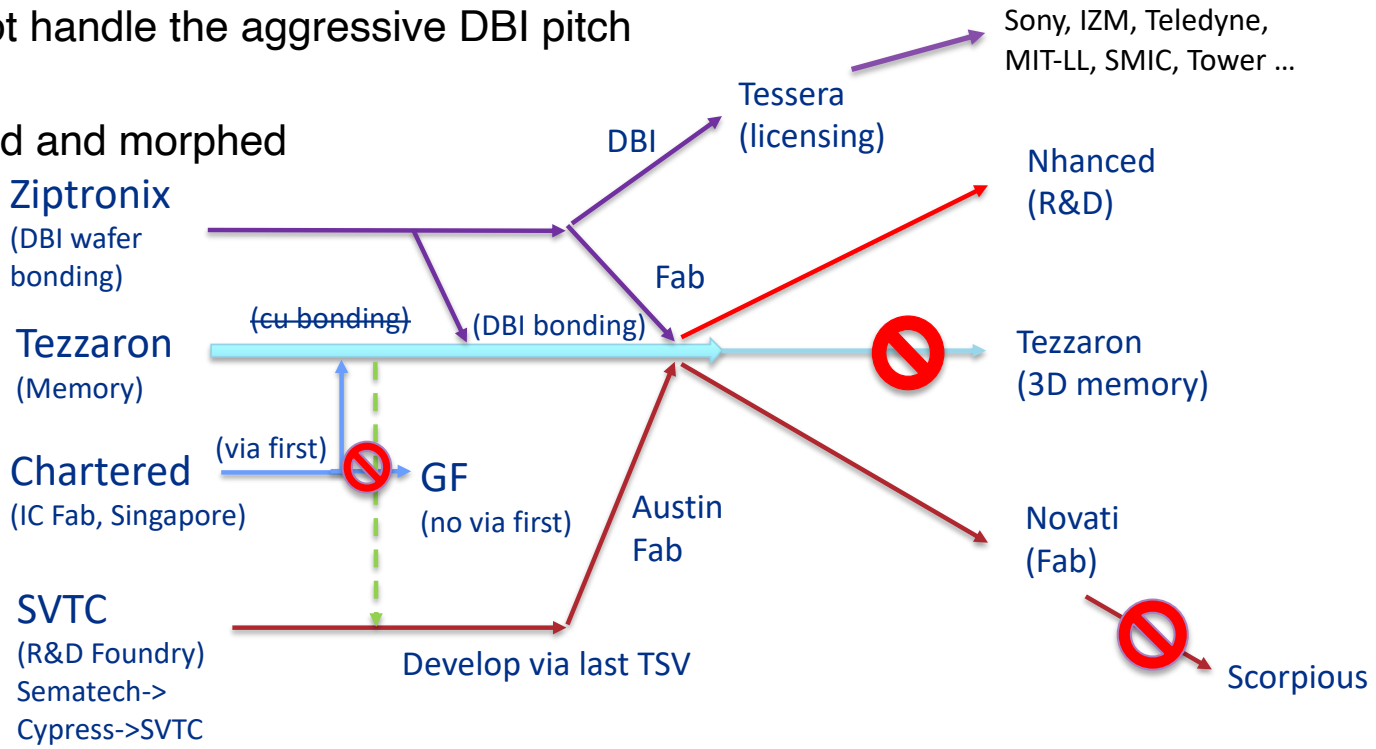
Our initial work with Tezzaron/Ziptronix was successful but:

- The initial Tezzaron cu-cu bonding process did not work
- Ziptronix DBI did work, and was used for the final wafers
- We achieved two tiers of wafer-wafer + 1 chip-wafer

The subsequent run included which included x-ray sensors and 3D track trigger designs used similar technologies - but the ground shifted under our feet:

- The Chartered 130 nm via-first TSV process was not longer available
- SVTC (bankrupt)->Novati tried to develop "via last" – this did not really work for our design
- Other vendors could not handle the aggressive DBI pitch we used
- Companies disappeared and morphed

The result was that the second run has not yet yielded any results.



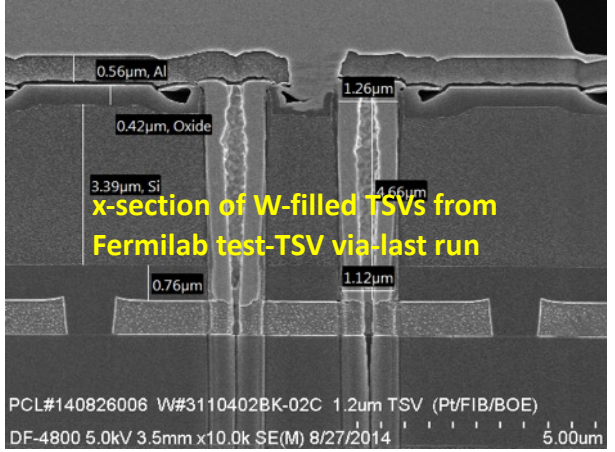
Possibilities and Challenges

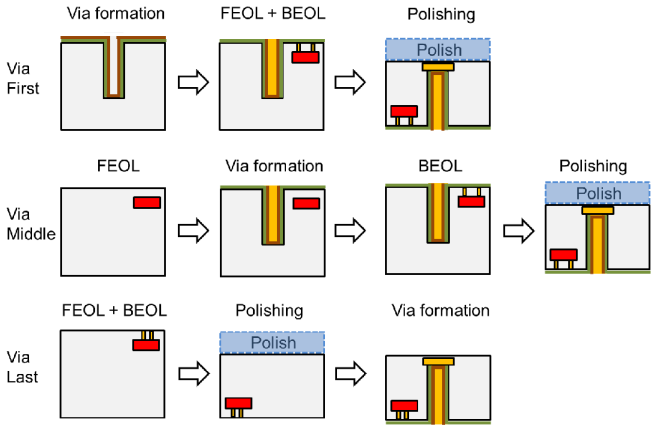
3D integration offers a number of possibilities

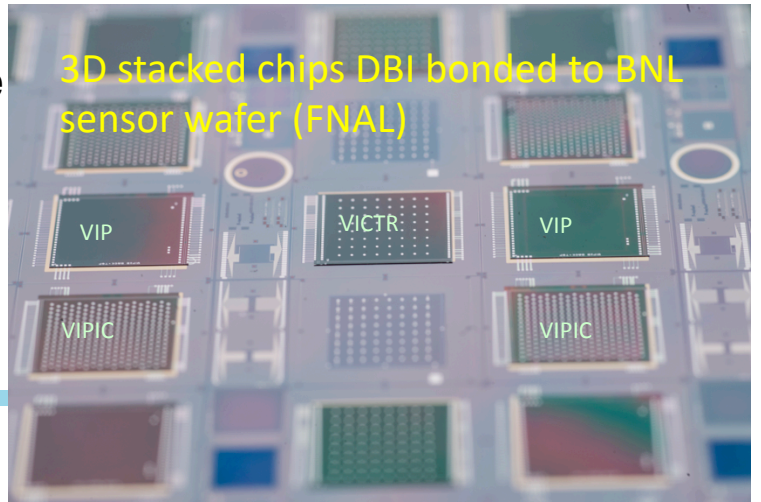
- Very fine pitch
- Multiple layers of electronics (analog/digital)
- Low noise (low capacitance interconnect, small pixels)
- Heterogeneous integration (different sensor, IC technologies in a stack)

Challenges

- Access/cost (Nhanced, MIT-LL, Tower/Jazz, Sandia, IZM, Skywater …)
- TSV integration (only from some foundries)
  - Via first, middle, last
- Die-to-wafer bonding
  - Small dicing shards are deadly -> plasma dice
- Multi-chip stack yield (Y^n) and test
- Design tools





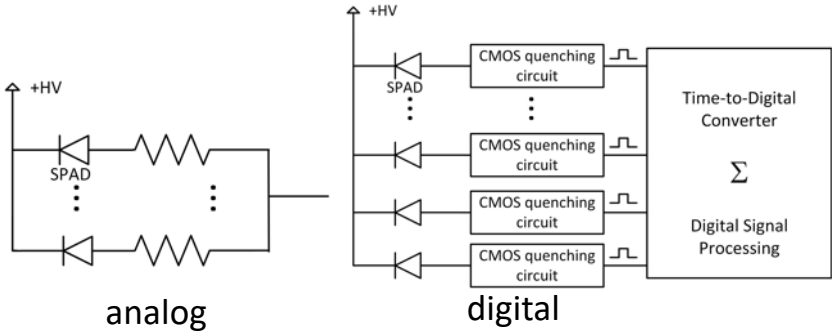


Applications – 3D SIPM

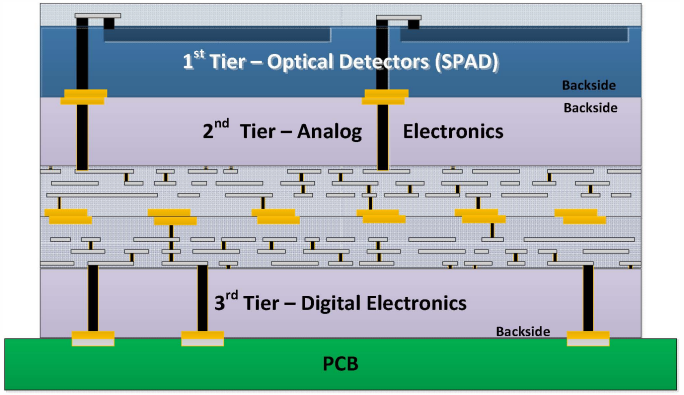
More sophisticated photodetector:

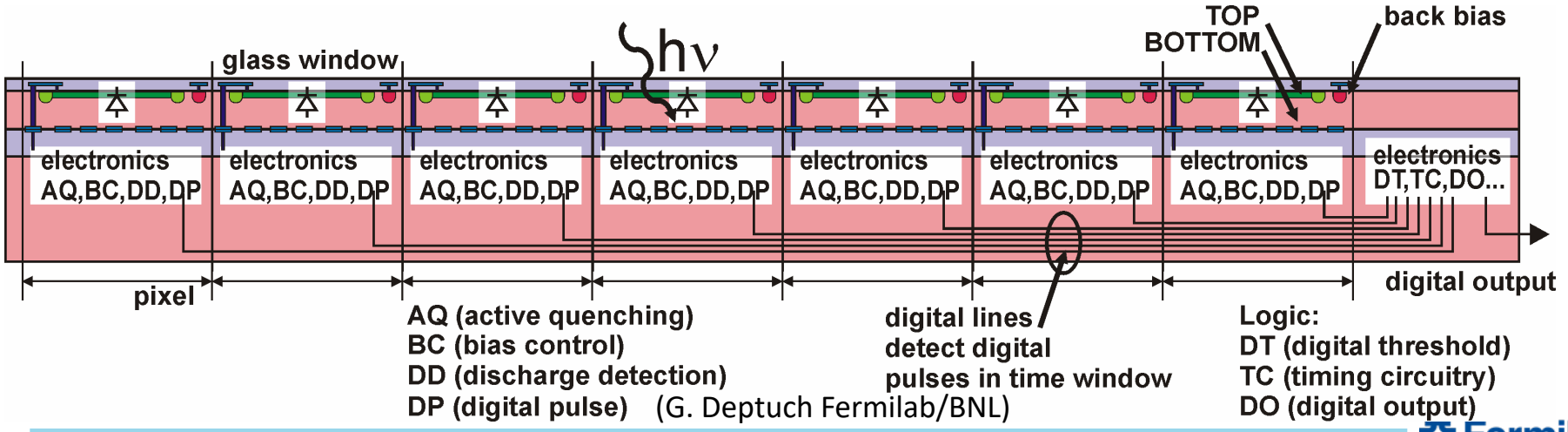
- Active quenching
- Interpixel communication
- Digital timing and discrimination
- Hit pixel counting
- Timing window
- Better fill factor – eliminate periphery
- Back side illumination

3D SIPM development at Sherbrooke, Canada with Teledyne/Dalsa also @ EFPL, Edinburgh, INFN, DESY/MPI, HPK, and MIT-LL (from Pratte et. al.)



(J.F Pratte Sherbrooke)





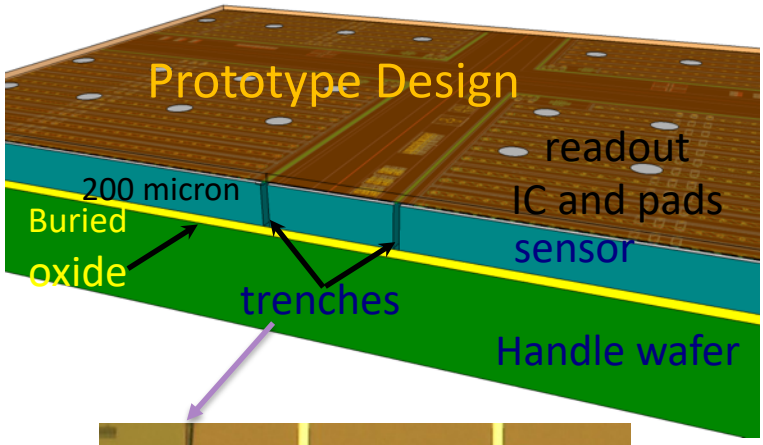
(G. Deptuch Fermilab/BNL)

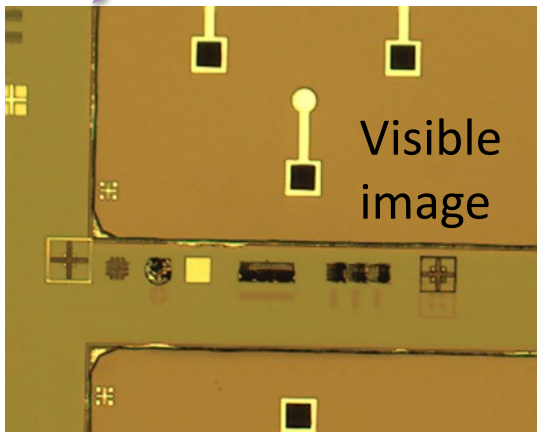
Applications - Edgeless array

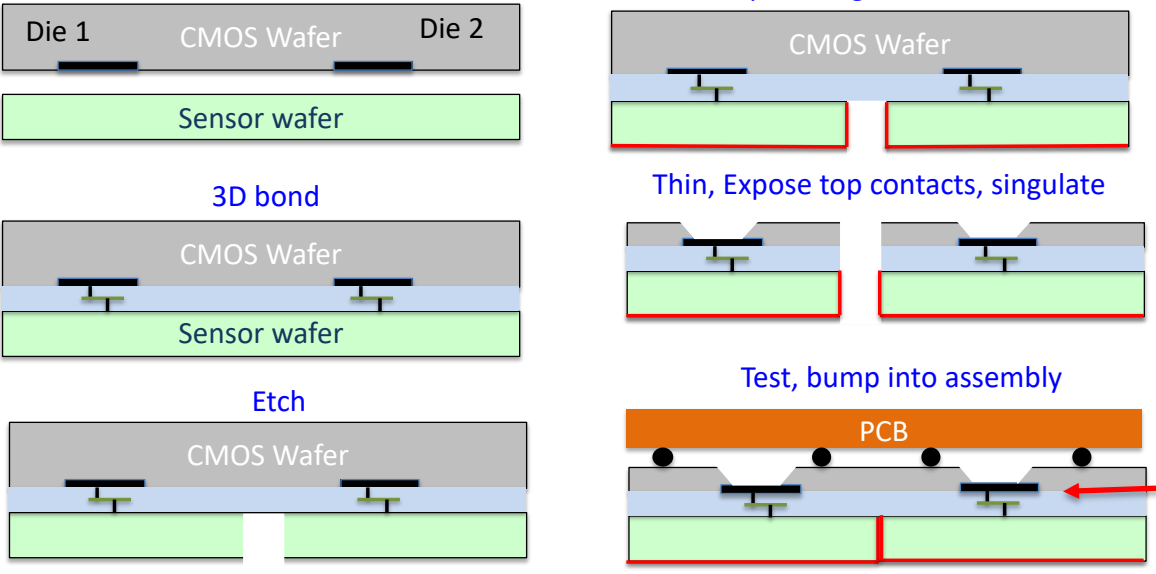
Combine active edge sensor technology with 3D electronics and oxide bonding with through-silicon vias to produce fully active tiles.

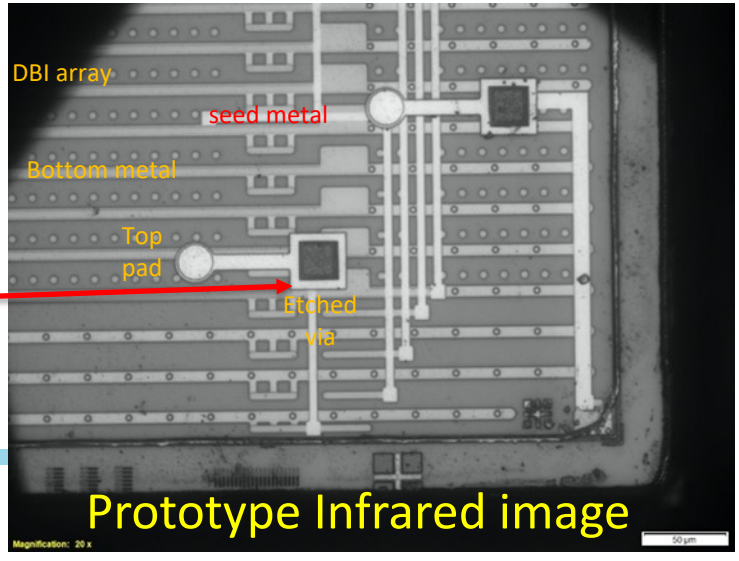
- These tiles can be used to build large area pixelated arrays with good yield and reasonable cost (test stack after 3D integration)
- Tiles can populate complex shapes with optimal tiling and low dead area, stitching not needed
- Only bump bonds are large pitch backside interconnects
- High density and geometrical flexibility

Prototypes fabricated, but not fully Assembled (broken in shipment)





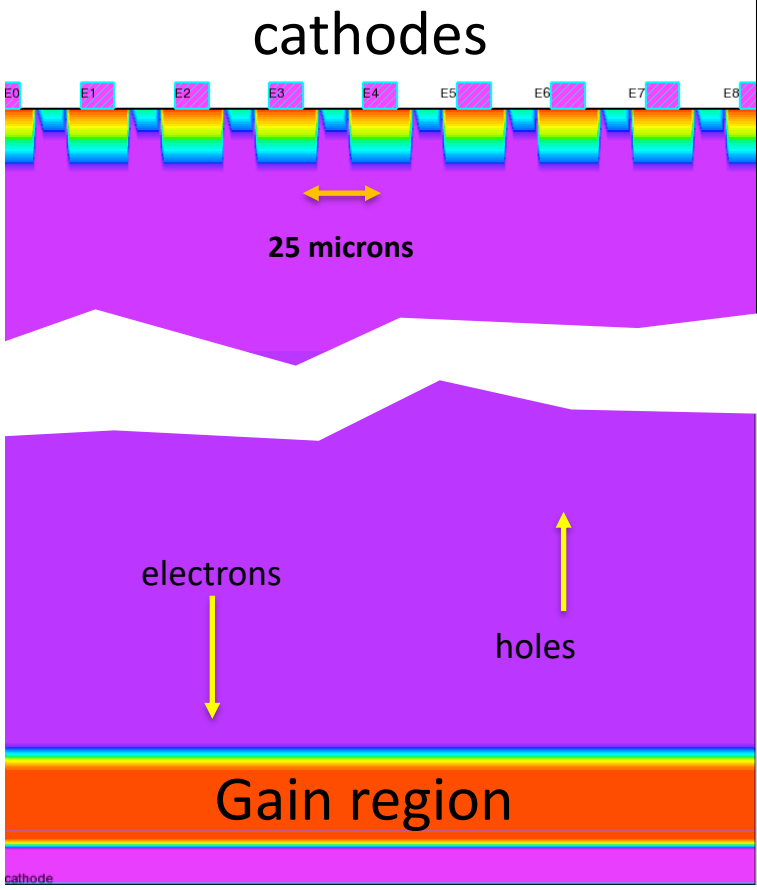


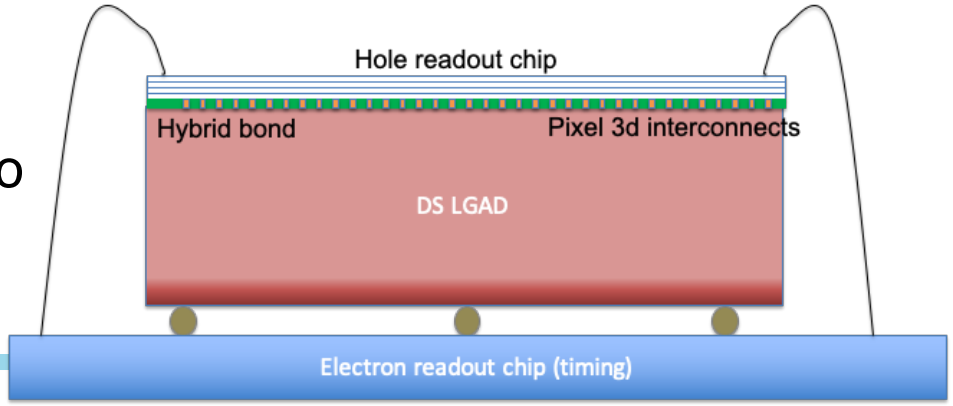


Applications – Double Sided LGAD

Low Gain Avalanche Diode with fine pixels on the hole-collecting side

- Anode can provide timing with coarse pitch
- Cathode subdivided into small pixels
  - Records “primary” hole collection, then holes from gain region – double peak that reflects charge deposition pattern
  - Lower power due to large signal from the gain layer
- Resulting current pattern can be used to measure angle and position.
- Top tier can survey a field of pixels – provide centroids, angle data …
- A thicker detector can be optimized to measure angle or charge deposit location

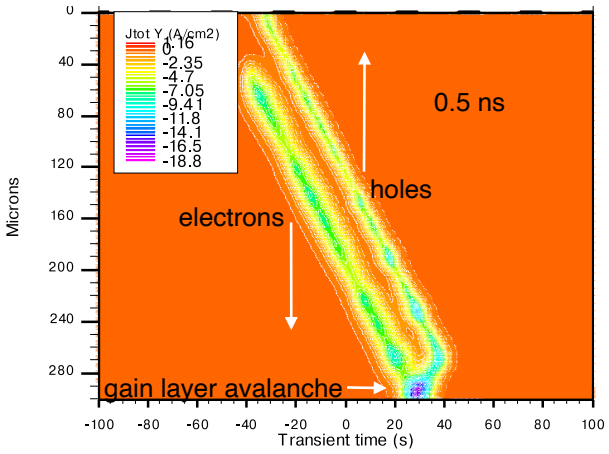


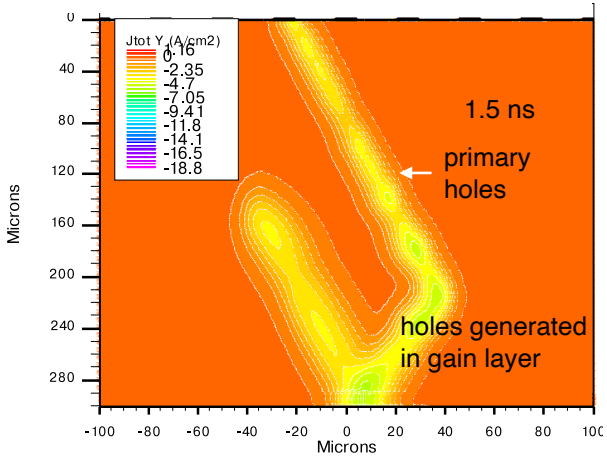


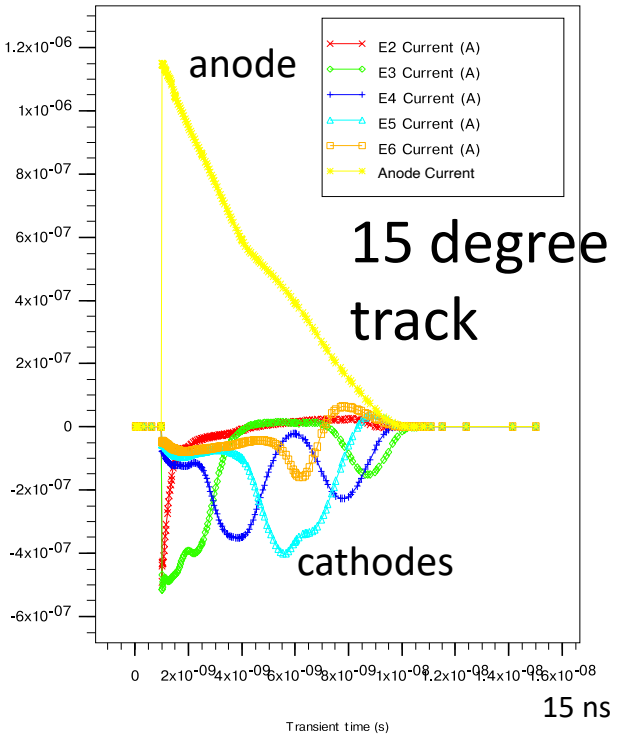
Double Sided LGAD Simulation

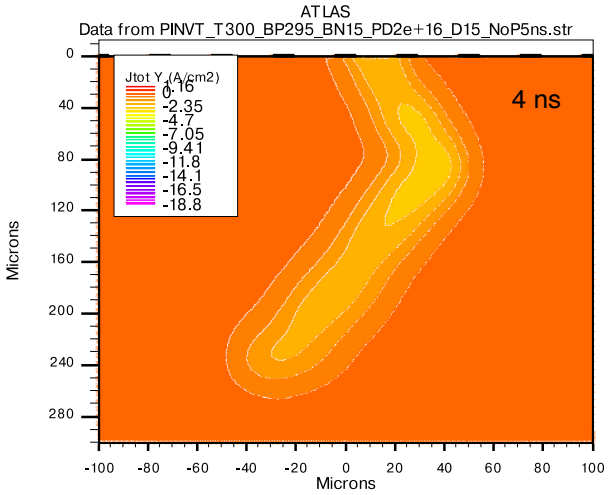
Use anode for timing, cathodes for pulse shape discrimination

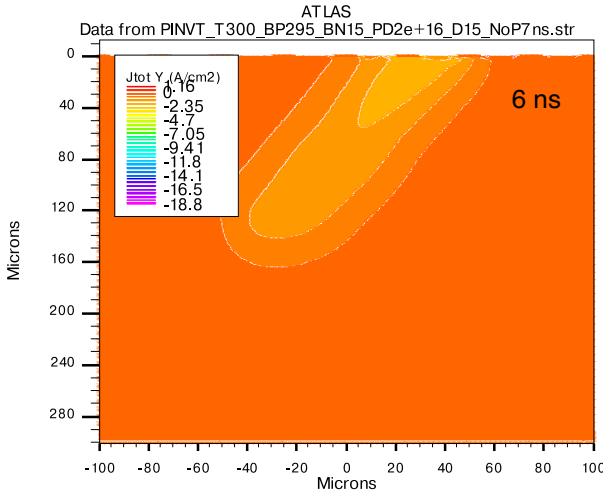
15 degree track detector internal current distributions

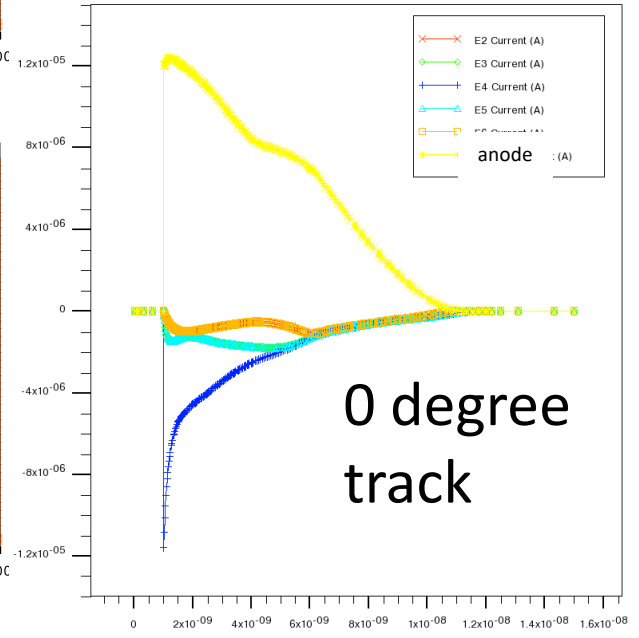








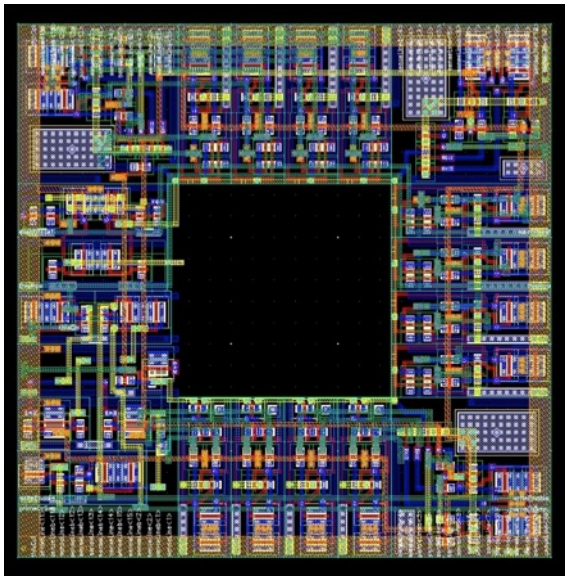




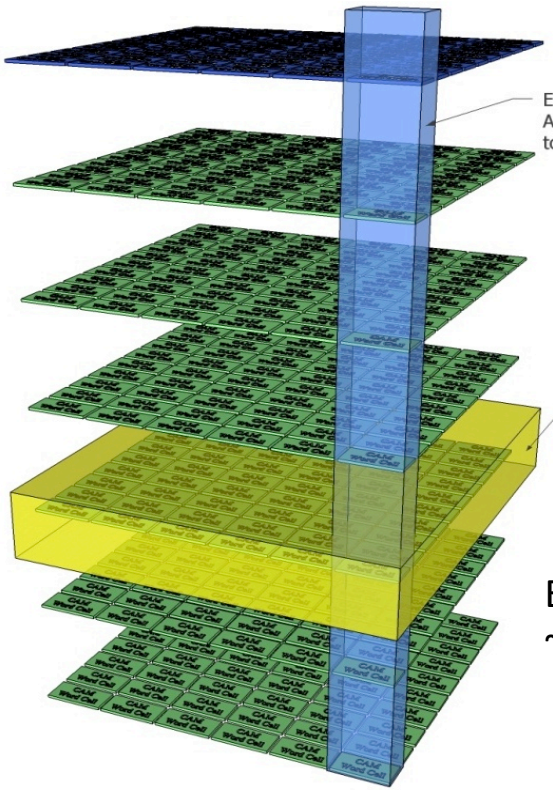
Application – 3D CAMS for trigger

The essence of VIPRAM is to divide the CAM trigger approach up into different tiers, maximizing pattern density while minimizing critical lengths and parasitics.

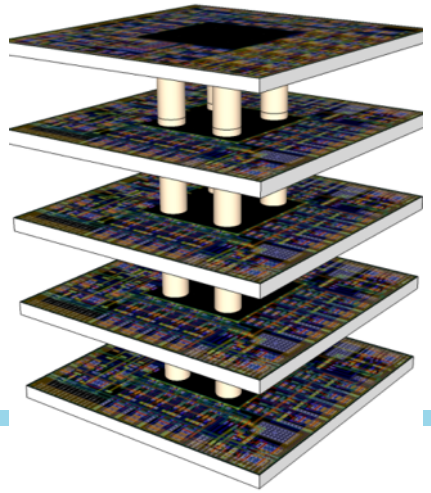
In 130nm



(Liu and Hoff (FNAL))



Each tier
~tracking layer



Fermilab

The Development Landscape

There are a variety of R&D projects utilizing 3D/TSV technology

SPADs in CMOS

- "Backside illuminated SPAD image sensor with 7.83 µm pitch in 3D-Stacked CMOS technology" T. Al Abbas et al, University of Edinburgh and STMicroelectronics, 2016 IEEE IEDM
- M.-J. Lee,..., E. Charbon, "High-performance back-illuminated three-dimensional stacked single-Photon Avalanche diode implemented in 45-nm CMOS technology"

Medipix and Timepix - AIDA program (via last)

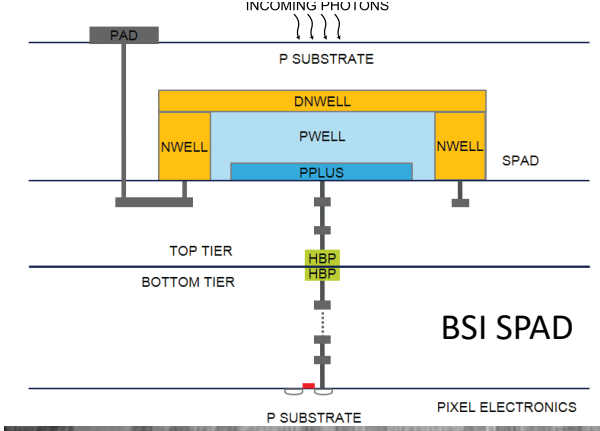
- M. Campbell et al, "Towards a new generation of pixel readout chips", 2016 JINST 11 C01007
- D. Henry et al., TSV Last for Hybrid Pixel Detectors: Application to Particle Physics and Imaging Experiments , (ECTC) (2013), p. 568
- X. Llopart, "Towards a new generation of Medipix and Timepix ASICs", FEE 2018, Orford, Canada

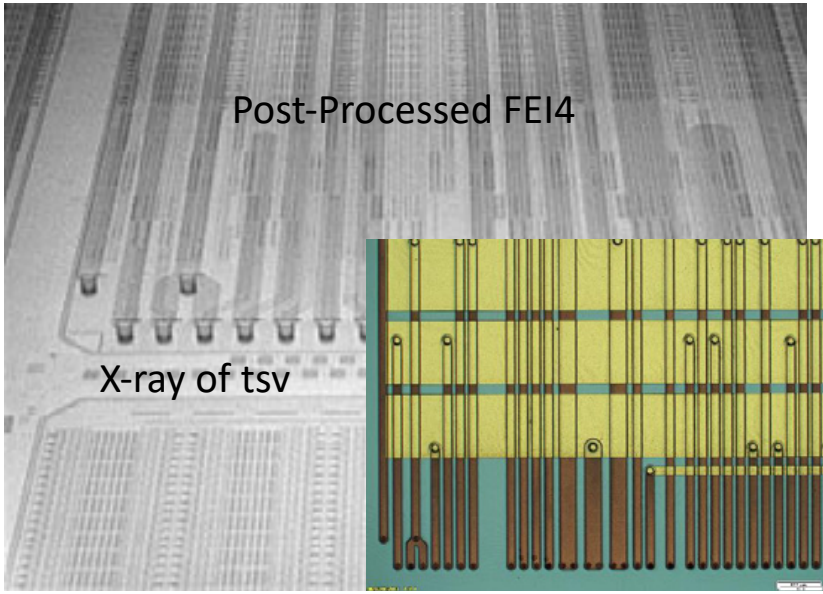
Collider

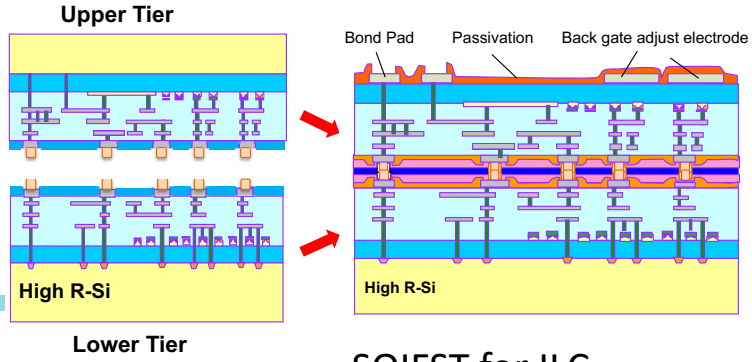
- Bonn - Through-Silicon Vias in 130 nm CMOS FE-I4 pixel readout chips
- M. Yamada et al., "3D Integrated Pixel Sensor with Silicon-on-Insulator Technology for the International Linear Collider Experiment," 2019 International 3D Systems Integration Conference

X-ray

- Flora, VIPIC-L, Faspax - G. Carini et al, "Hybridized MAPS with in-pixel A-to-D conversion readout ASIC for high-throughput imaging", ULITIMA 2018, Argonne National Lab.
- XIMOS – CMOS sensor with peripheral TSV
- The TSV process in the hybrid pixel detector for the High Energy Photon Source, NIM A, Volume 980, 2020

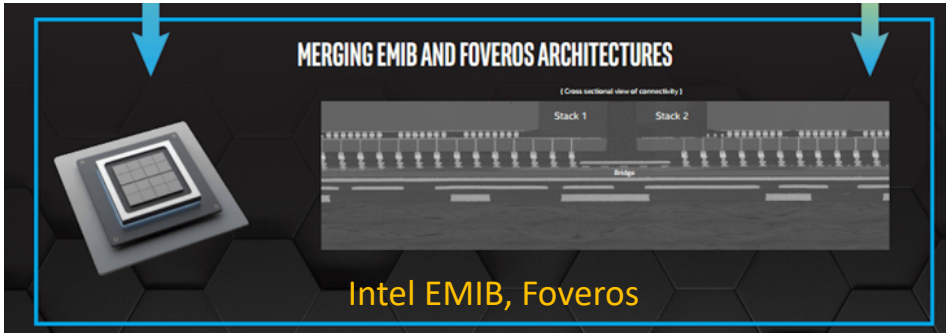






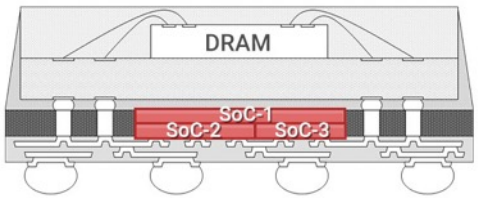
SOIFST for ILC

2.5D Interposers & Chiplets

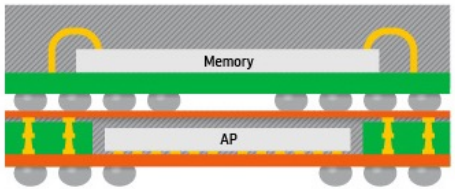


Known good die can be combined on an active or passive interposer, with or without TSVs

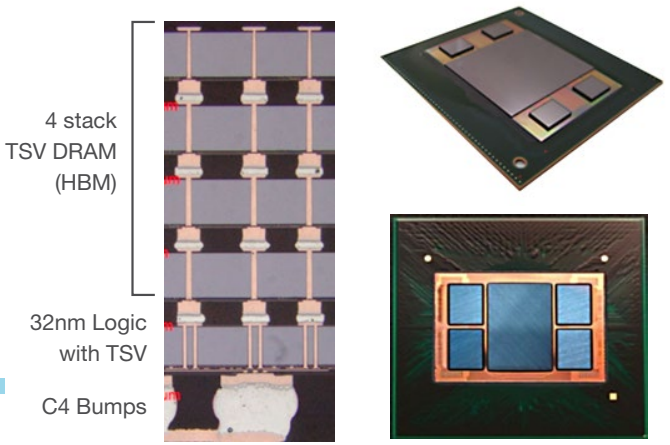
- Interconnect on silicon or glass substrate
  - Fine pitch, fast, dense
- Uses on microbump arrays + hybrid bonding
- Build complex assemblies with specialized ASICs
- A better way to implement
  - Front end amplification
  - Optical data transfer
  - Power conversion
  - Data concentration and filtering
  - Trigger generation
- Could provide possibly more elegant solution for i.e. the CMS PS module (4 chip-on-flex hybrids)



TSMC SoIC

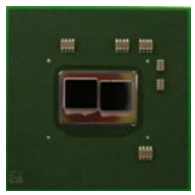


Samsung PoP



3D Logic + HBM

2.5D — Si Interposer, HBM



3D Package

Global Foundries

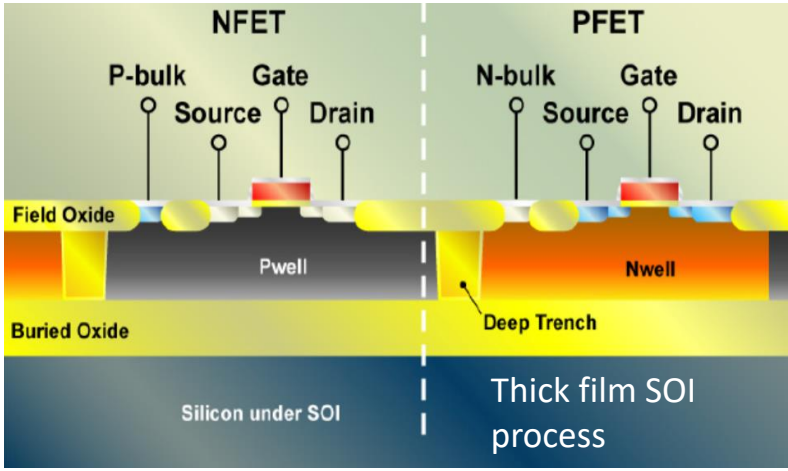
TSV Si Interposer		Availability
Full Reticle	26x33mm²	●
Stitched Interposer	>1300 mm²	○
10:1 Aspect Ratio TSV	10um Dia./ 100um Depth	●
TSV Pitch	40um	●
L/S	0.8/ 0.8um	●
Deep Trench Capacitors	400nF/mm²	●
BEOL Layers	4 Metal Layers	●
	5 Metal Layers	○

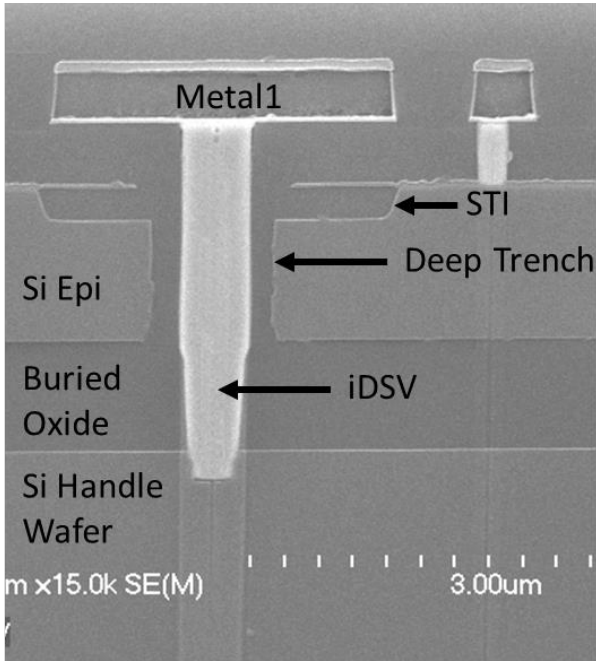
● *Available* ○ *In Development*

Access and Comments

Comments on the “cutting edge”

- Companies can appear and disappear (with access and capabilities)
- We (HEP) are more willing to take risks than most other customers and can provide valuable service as “first adopters”
- We benefited from aggressive ILC goals and detector R&D funds
- Labs (for example BNL, MIT-LL, SLAC, FNAL) are capable and interested, but costly. R&D funds and people are limited
- Access to foundries is crucial for much of the work. All major foundries now have 3D technology, – a few are willing to talk.
- TCAD and simulation tools are powerful and underutilized (in the US)
- Close collaboration with engineering groups is essential
- University semiconductor labs can be a great resource, but help can be limited. Student participation is very important.
- Funding can be obtained from SBIRs – that is what the program is for. But:
  - Companies can overstate their capabilities – be skeptical
  - You need to provide expertise to get what you want





Tower/Jazz TSV process

Ecosystem needs

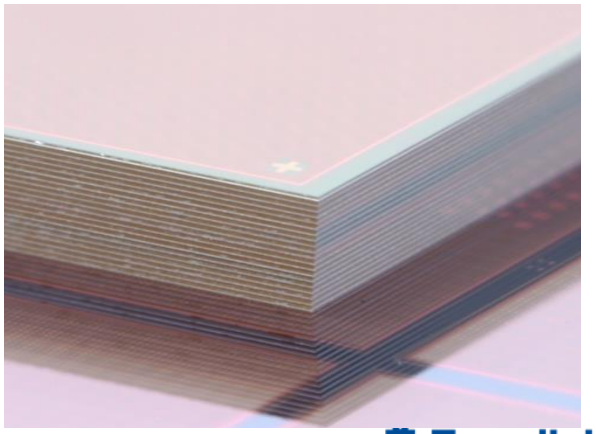
- TSV availability in affordable nodes with high aspect ratio and fine pitch
  - Foundry Multiproject runs (Europractice/CMP 3D TSV(last) and micro-bumps)
    - IP protection
  - Viable via-last processes – not one-offs
  - Post-process hybrid bonding availability (Nhanced, others … getting there)
- Chip-chip and chip-wafer bonds (yields)
- Interposer and chiplet design and assembly (old-style hybrids)
- 3D compliant design tools, standard cells
- Testing 3D structures

Package Roadmap

GF Technology Node (nm)

	180	130	65	55	45	40	32	28	22	14	12
QFN	●	●	●	●	●	●	●	●			
FBGA	●	●	●	●	●	●	●	●	○		
fcCSP (SnAg)	●	●	●	●	●	●	●	●	●	●	○
fcCSP (Cu)	●	●	●	●	●	●	●	●	●	●	○
FCBGA (SnAg)	●	●	●	●	●	●	●	●	○	●	○
FCBGA (Cu)	●	●	●	●	●	●	●	●	○	●	○
WLCSP	●	●	●	●	●	●	●	●	●		○
FOWLP	●	●	●	●	●	●	●	●	●		
TSV			●				●			●	○
2.5D							●	●		○	○
3D							●			○	○

● *Available* ○ *In Development*



20 die x 50µ hybrid bonded stack

Conclusions

- Now is the time when detector R&D should ramp up for the next generation of experiments.
  - Experimental challenges are not getting any easier
- There are many promising technologies becoming available that have the potential to revolutionize the next generations of experiments
  - Investment with delayed payoffs
- We need to think about what technologies will be available 10 years from now and start developing the tools to use them

The reach of our experiments has always been defined by the instrumentation we use. We need to continue to invest.

Collaborators/Companies

Ziptronix, Tezzaron, Nhanced, Novati/SVTC, MIT-LL, RTI, KEK, T-Micro, American Semiconductor, Cactus Materials, Tower/Jazz, On Semiconductor, Voxtel, CVI

Cornell, BNL, SLAC, LBNL, FNAL, KEK, Argonne, + 3D consortium

Applications – Induced currents

Jitter

$$\sigma_t \sim \sigma_{noise}\left(\frac{\partial V}{\partial t}\right) \sim t_r\left(\frac{Noise}{Signal}\right)$$

Front end noise

$$\sigma_n^2 = \frac{C_L^2(4ktA)}{g_m t_a}$$

Time resolution

$$\sigma_t \sim \frac{C_L}{\sqrt{g_m t_a}} \frac{\sqrt{t_a^2 + t_d^2}}{Signal}$$

3D allows for small pixels with small associated load capacitance. Small pixels with ~25x smaller capacitance should have similar timing performance to LGADs.

- Should be more radiation hard, but more power with denser electronics

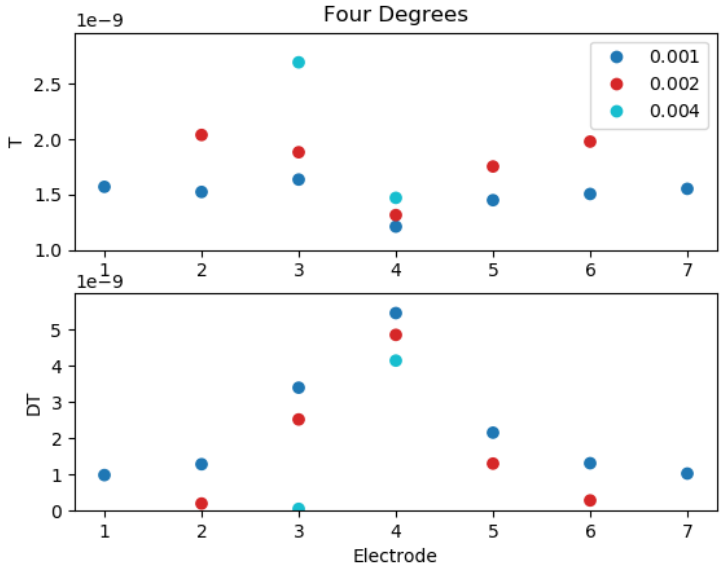
The current pulse reflects charge motion deep in the detector

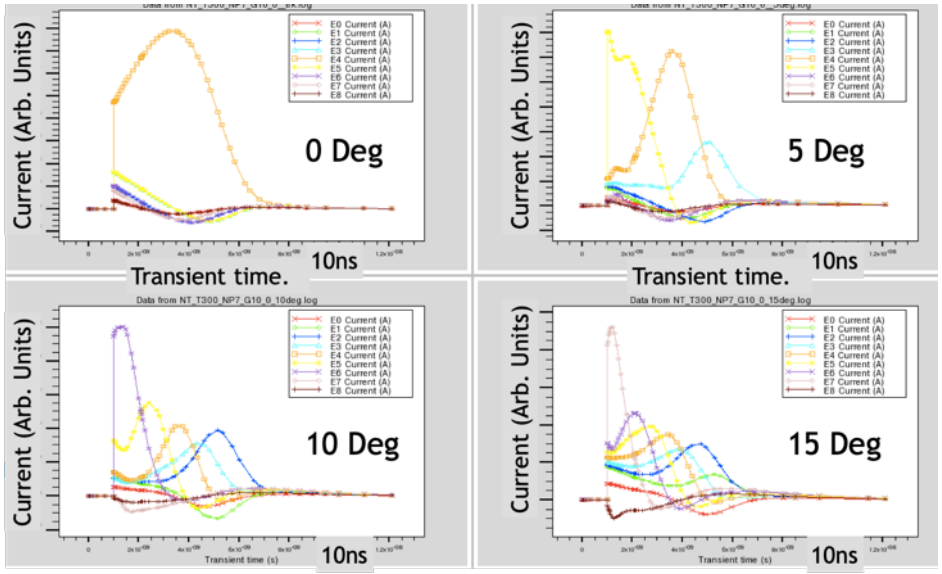
- Can use the current pulse to measure track angle, depth of charge deposition
- Depends sensitively on the "weighting field"

$$i = -q\vec{E}_w \times \vec{v}$$

$$Q_s = \int i\,dt = q\int \vec{E}_w d\vec{x}$$

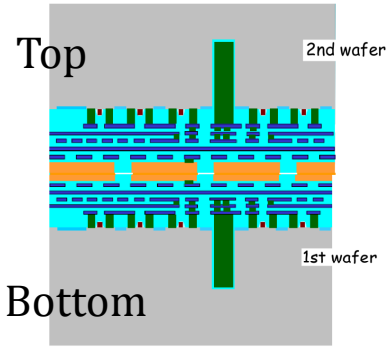
$$Q_{1\to 2} = q(V_{w2} - V_{w1})$$

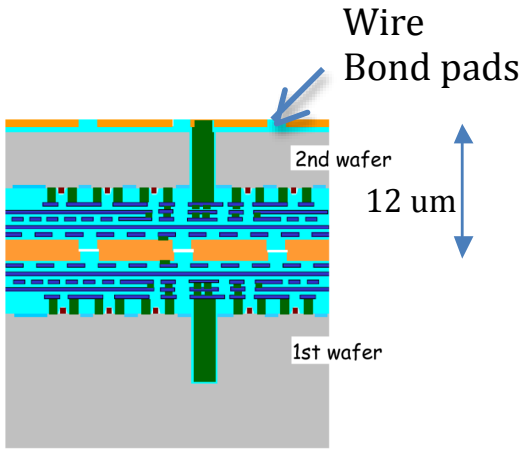


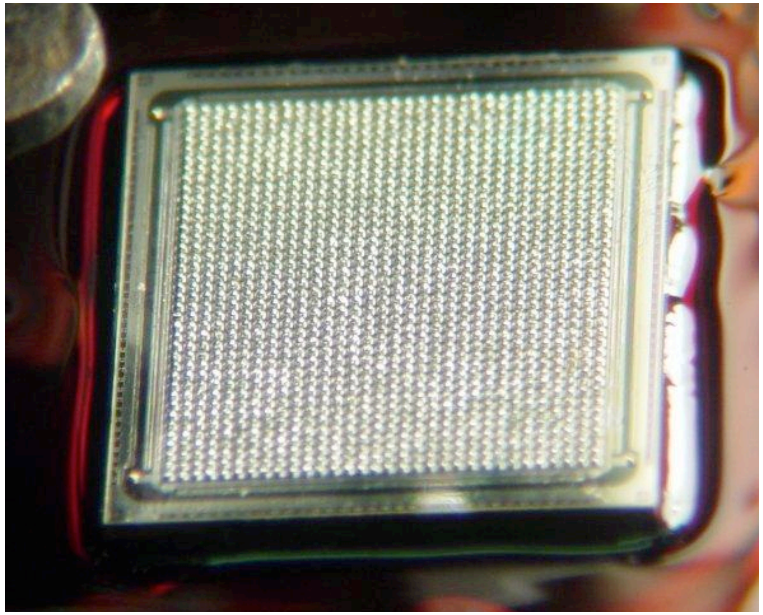


Two-Tier Devices

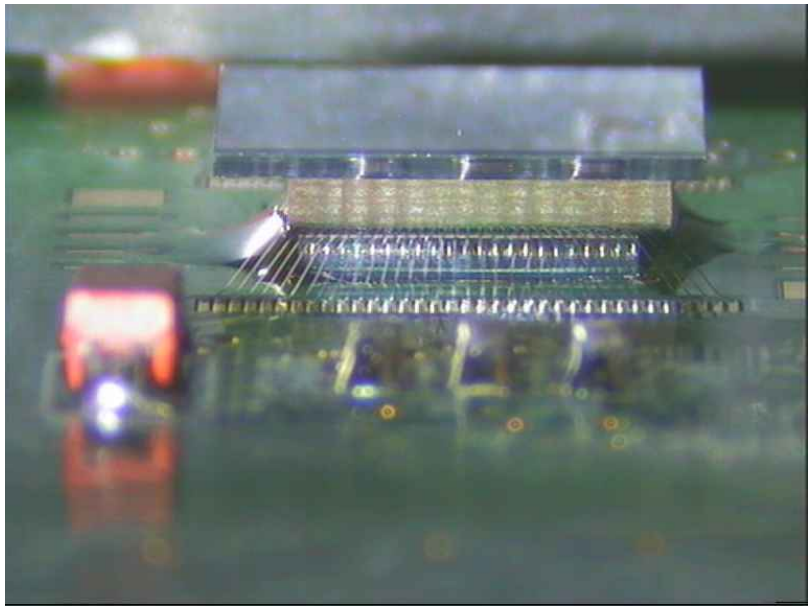
- Final two-tier face-to-face bonded wafers were delivered in 2013
- VICTR and VIPIC wafers were tested, both bare and with bump bonded sensors.







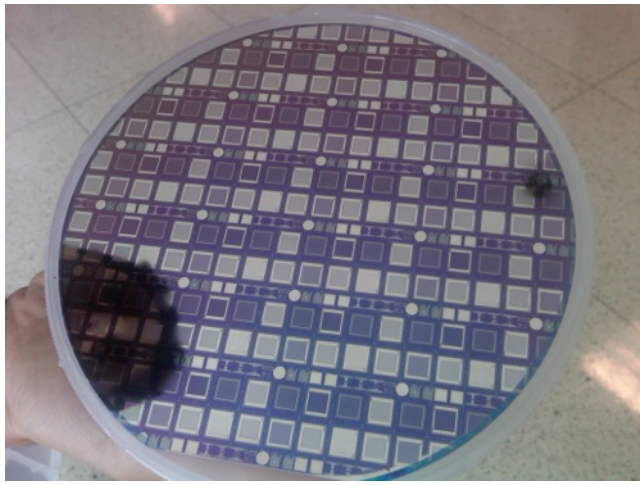
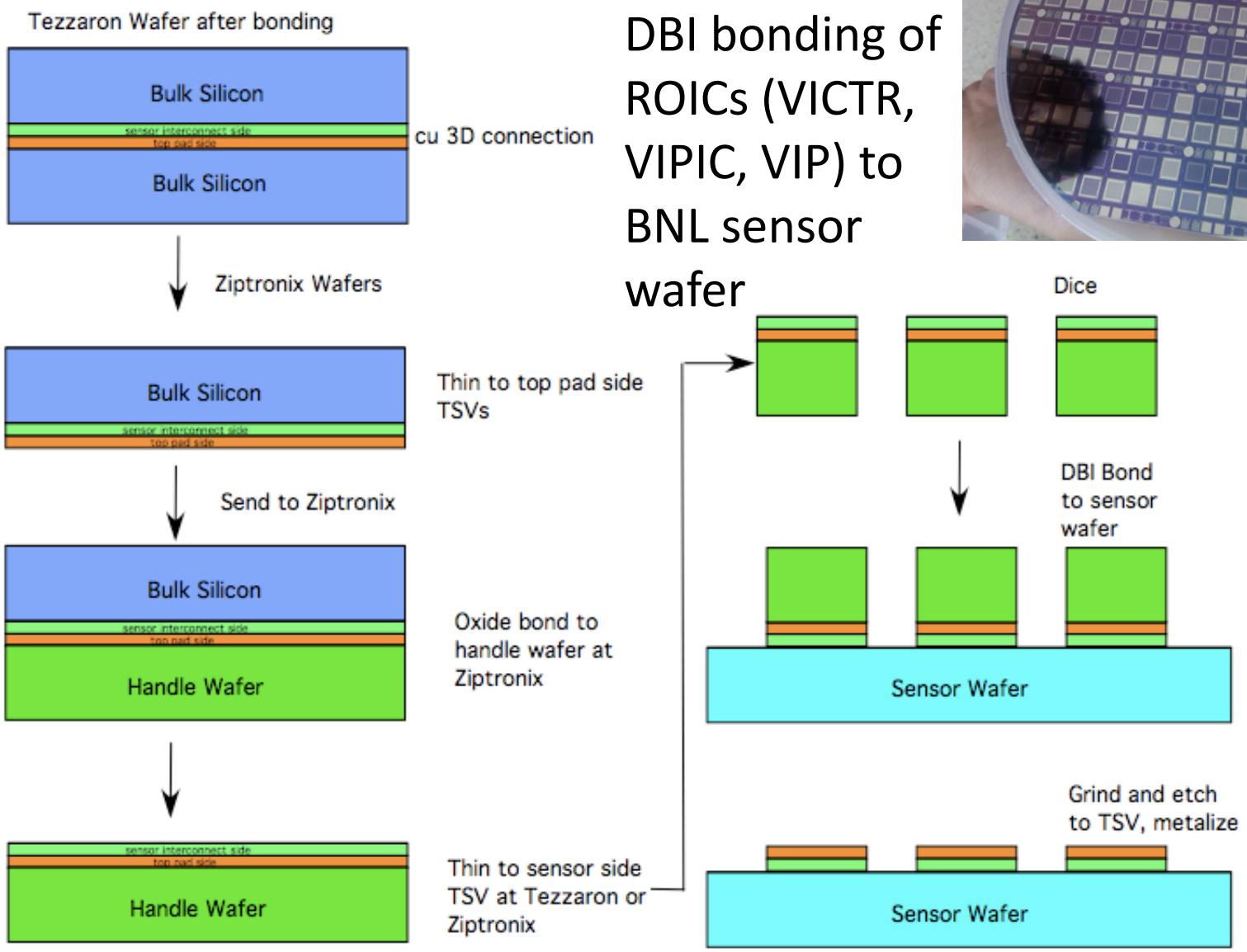
VIPIC with bumps



VICTR with top sensor and interposer

Fermilab

Chip-to-Wafer bond



DBI bonding of ROICs (VICTR, VIPIC, VIP) to BNL sensor wafer